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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,923	03/10/2004	Shoichi Furuhata	FUJI:300	3352

37013 7590 07/27/2005

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,923	FURUHATA, SHOICHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *10-13* is/are withdrawn from consideration.

5)☒ Claim(s) *6 and 9* is/are allowed.

6)☒ Claim(s) *1-5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 06/30/2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by NISHIZAWA ET AL. (5,663,582).

With regard to claims 1-3, Nishizawa et al. discloses a semiconductor wafer comprising a first conduction type low concentration impurity layer 12 formed beneath a principal face of a wafer to a predetermined depth; a first conduction type high concentration impurity layer 11 having an impurity concentration of $5X10^{19}$/cc (and thus, inherently, resistance value not higher than 0.05 Ω•cm, note figure 6 of Kroger 4,544,937) directly (that is to say, in direct contact with) underlying said low concentration impurity layer 12; and a first conduction type high concentration impurity diffusion region 23 (note, column 6 line 46, that region 23 may reach all the way to region 11, even though figure 6 does not depict this fea-

ture) having a lattice-shaped pattern on said wafer, said high concentration impurity diffusion region 23 extending from the principal face of the wafer to said high concentration impurity layer 11, wherein said high concentration impurity diffusion region 23 has a width larger than that of the cutting allowance for the dicing along the dicing lines A-A. Note figures 6,5, and 2, column 4 lines 20-45, and column 6 lines 27-49 of Nishizawa et al.

With regard to claims 4 and 5 Nishizawa et al. discloses a semiconductor wafer comprising a first conduction type low concentration impurity layer 12; a first conduction type high concentration impurity layer 11 having an impurity concentration of $5X10^{19}$/cc (and thus, inherently, resistance value not higher than 0.05 Ω•cm, note figure 6 of Kroger 4,544,937) directly (that is to say, in direct contact with) underlying said low concentration impurity layer 12; and a first conduction type high concentration impurity diffusion region 23 (note, column 6 line 46, that region 23 may reach all the way to region 11, even though figure 6 does not depict this feature) that extends from the upper surface of said low concentration impurity layer 12 to said high concentration impurity layer 11, said high concentration impurity diffusion region 23 being positioned at the outer edge of an element region 13-20 having a semiconductor element 16B formed therein, wherein said high concentration impurity diffusion region 23 comprises a portion or the entirety of dicing regions A-A on a wafer containing said device. Note figures 6,5, and 2, column 4 lines 20-45, and column 6 lines 27-49 of Nishizawa et al.

B. Claims 4,7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by ONISHI ET AL. (2001/0028083).

Onishi et al. discloses a semiconductor wafer comprising a first conduction type low concentration impurity layer 20B; a first conduction type high concentration impurity layer 11 directly (that is to say, in direct contact with) underlying said low concentration impurity layer 20B; and a first conduction type high (relative to low concentration impurity layer 20B) concentration impurity diffusion region 24 that extends from the upper surface of said low concentration impurity layer 20B to said high concentration impurity layer 11, said high concentration impurity diffusion region 24 being positioned at the outer edge of an element region 20 having a semiconductor element 22 formed therein, wherein said high concentration impurity diffusion region 24 comprises a portion or the entirety of dicing regions on a wafer containing said device, wherein said high concentration impurity diffusion region 24 electrically connects said high concentration impurity layer 11 with at least one electrode 25 positioned above said low concentration impurity layer 20B, by being electrically connected with at least one electrode 25 formed on the upper surface of said low concentration impurity layer 20B. Note figures 1a-b and paragraphs 0054-0055 and 0059 of Onishi et al.

Allowable Subject Matter

3. Claims 6 and 9 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising a first conduction type low concentration impurity layer; a first conduction type high concentration impurity layer underlying said low concentration impurity layer; and a first conduction type high concentration impurity diffusion region that extends from the upper surface of said low concentration impurity layer to said high concentration impurity layer, said diffusion region being positioned at the outer edge of an element region having a semiconductor element formed therein, wherein said diffusion region comprises a portion or the entirety of dicing regions on a wafer containing said device, wherein said element region comprises a power semiconductor element and a control circuit for controlling said power semiconductor element, as recited in claim 6, or wherein said high concentration impurity layer has a resistance value not higher than 0.05 Ω•cm and a plurality of high concentration impurity diffusion regions connect said high concentration impurity layer to a plurality of electrodes positioned above said low concentration impurity layer, as recited in claim 9.

Response to Arguments

4. Applicant's arguments with respect to claims 1-5,7, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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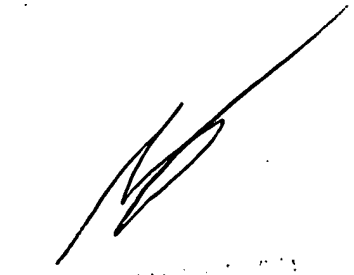

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TECHNOLOGY CENTER 2800